AMENDMENTS TO THE CLAIMS

Listing of Claims

1. (Currently Amended) A drive circuit outputting to an output node ~~(N2)~~ a potential ~~(VO)~~ corresponding to an input potential ~~(VI)~~, comprising:

a first sub-drive circuit including:

a first transistor ~~(10)~~ of a first conductivity type connected between a first power supply potential ~~(VDD)~~ line and ~~said output~~ a first node;

a second transistor ~~(9)~~ of the first conductivity type having a gate and a first electrode connected to a gate of said first transistor ~~(10)~~, and a second electrode connected to a second ~~first~~ node ~~(N9)~~;

a third transistor ~~(8)~~ connected in series with said second transistor ~~(9)~~ between second and third power supply potentials ~~(VDD, GND) lines~~; and

a first differential amplifier ~~(2)~~ for regulating a gate potential of said third transistor ~~(8)~~ to match a potential at said second ~~first~~ node ~~(N9)~~ with said input potential ~~(VI)~~;

a second sub-drive circuit including: a fourth transistor of a second conductivity type connected between a fourth power supply potential line different from said first power supply potential and a third node;

a fifth transistor of a second conductivity type having a gate and a first electrode connected to a gate of said fourth transistor, and a second electrode connected to a fourth node;

a sixth transistor connected in series with said fifth transistor between said second and third power supply potential lines; and

a second differential amplifier for regulating a gate potential of said sixth transistor to match a potential at said fourth node with said input potential;

a first offset compensation circuit for eliminating an offset voltage of said first sub-drive circuit and connecting said first node to said output node; and

a second offset compensation circuit for eliminating an offset voltage of said second sub-drive circuit and connecting said third node to said output node.

2. (Currently Amended) The drive circuit according to claim 1, wherein said third transistor ~~(8)~~ is connected between said second power supply potential ~~(VDD)~~ line and the first electrode of said second transistor ~~(9)~~, ~~and~~

said first sub-drive circuit ~~said drive circuit~~ further includes ~~comprises~~ a current limiting element ~~(11)~~ connected between said second ~~first~~ node ~~(N9)~~ and said third power supply potential ~~(GND)~~ line.

3. (Currently Amended) The drive circuit according to claim 2, wherein said first sub-drive circuit further includes ~~comprising~~ a switching element ~~(76)~~ connected in parallel with said current limiting element ~~(11)~~ to conduct in a pulsing manner with prescribed timing ~~as said input potential (VI) is changed from said second power supply potential (VDD) towards said first power supply potential (GND)~~.

4. (Currently Amended) The drive circuit according to claim 1, wherein said third transistor ~~(35)~~ is connected between said second ~~first~~ node ~~(N34)~~ and said third power supply potential ~~(GND)~~ line, ~~and~~

said first sub-drive circuit ~~said drive circuit~~ further includes ~~comprises~~ a current limiting element ~~(32)~~ connected between said second power supply potential ~~(VDD)~~ line and the first electrode of said second transistor ~~(34)~~.

5. (Currently Amended) The drive circuit according to claim 4, wherein said first sub-drive circuit further includes ~~comprising~~ a switching element ~~(81)~~ connected in parallel with said current limiting element ~~(32)~~ to conduct in a pulsing manner with prescribed timing ~~as said input potential (VI) is changed from said third power supply potential (GND) towards said second power supply potential (VDD)~~.

Claims 6-10 (Canceled)

11. (Currently Amended) The drive circuit according to claim 1 ~~10~~, wherein said third transistor ~~(8)~~ is connected between said second power supply potential ~~(VDD)~~ line and the first electrode of said second transistor ~~(9)~~, ~~and~~

said sixth transistor ~~(67)~~ is connected between said third power supply potential ~~(GND)~~ line and the first electrode of said fifth transistor ~~(57)~~, ~~and~~

said first sub-drive circuit ~~drive circuit~~ further includes ~~comprises~~: a first current limiting element ~~(11)~~ connected between said second ~~first~~ node ~~(N9)~~ and said third power supply potential ~~(GND)~~ line, and

said second sub-drive circuit further includes a second current limiting element ~~(66)~~ connected between said fourth ~~second~~ node ~~(N56)~~ and said second power supply potential ~~(VDD)~~ line.

12. (Currently Amended) The drive circuit according to claim 1 ~~10~~, wherein said third transistor ~~(35)~~ is connected between said second ~~first~~ node ~~(N34)~~ and said third power supply potential ~~(GND)~~ line,

said sixth transistor ~~(56)~~ is connected between said fourth ~~second~~ node ~~(N57)~~ and said second power supply potential ~~(VDD)~~ line, ~~and~~

said first sub-drive circuit ~~said drive circuit~~ further includes ~~comprises~~: a first current limiting element ~~(32)~~ connected between said second power supply potential ~~(VDD)~~ line and the first electrode of said second transistor ~~(34);~~ , and

said second sub-drive circuit further includes a second current limiting element ~~(59)~~ connected between said third power supply potential ~~(VDD)~~ line and the first electrode of said fifth transistor ~~(57)~~.

13. (Currently Amended) The drive circuit according to claim 1 ~~10~~, wherein said third transistor ~~(8)~~ is connected between said second power supply potential ~~(VDD)~~ line and the first

electrode of said second transistor (9),

said sixth transistor (56) is connected between said fourth second node (N56) and said second power supply potential (VDD) line,

said first sub-drive circuit said drive circuit further includes comprises: a first current limiting element (11) connected between said second first node (N9) and said third power supply potential (GND) line; , and

said second sub-drive circuit further includes a second current limiting element (59) connected between said third power supply potential (GND) line and the first electrode of said fifth transistor (57).

14. (Canceled)

15. (Currently Amended) The drive circuit according to claim 1 14, wherein one electrode of said first transistor (10) and one electrode of said fourth transistor (58) are connected to third and fourth nodes (N10, N60), respectively, instead of being connected to said output node (N2), said first offset compensation circuit (12, 111a, S1a-S4a) includes:

a first current limiting element (12) connected between said first third node (N10) and a sixth power supply potential (GND) line;

a first capacitor (111a);

a first switching circuit (S1a, S2a) for providing said input potential (VI) to one electrode of said first capacitor (111a) and connecting the other electrode of said first capacitor (111a) to said first third node (N10);

a second switching circuit (S3a) for providing said input potential (VI) to the other electrode of said first capacitor (111a) and providing, instead of said input potential (VI), a potential of the one electrode of said first capacitor (111a) to said first differential amplifier (2); and

a third switching circuit (S4a) for providing a potential at said first third node (N10) to said output node (N2), and

said second offset compensation circuit (60, 111b, S1b-S4b) includes:

a second current limiting element (60) connected between said third fourth node (N60)

and a seventh power supply potential ~~(VDD)~~ line;

a second capacitor ~~(111b)~~;

a fourth switching circuit ~~(S1b, S2b)~~ for providing said input potential ~~(VI)~~ to one electrode of said second capacitor ~~(111b)~~ and connecting the other electrode of said second capacitor ~~(111b)~~ to said third ~~fourth~~ node ~~(N60)~~;

a fifth switching circuit ~~(S3b)~~ for providing said input potential ~~(VI)~~ to the other electrode of said second capacitor ~~(111b)~~ and providing, instead of said input potential ~~(VI)~~, a potential of the other electrode of said second capacitor ~~(111b)~~ to said second differential amplifier ~~(2)~~; and

a sixth switching circuit ~~(S4b)~~ for providing a potential at said third ~~fourth~~ node ~~(N60)~~ to said output node ~~(N2)~~.

16. (Currently Amended) The drive circuit according to claim 1, wherein said first differential amplifier ~~(2)~~ includes:

seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6) of a first conductivity type~~ having gates receiving the input potential ~~(VI)~~ and a potential at said second ~~first~~ node ~~(N9)~~, respectively, and first electrodes connected to each other;

ninth and tenth ~~sixth and seventh~~ transistors ~~(3, 4)~~ of a conductivity type different from that of said seventh and eighth transistors, connected between a fourth power supply potential ~~(VDD)~~ line and second electrodes of said seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6)~~, respectively, and having gates connected to the second electrode of said eighth ~~fifth~~ transistor ~~(6)~~; and

a current limiting element ~~(7)~~ connected between the first electrodes of said seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6)~~ and a fifth power supply potential ~~(GND)~~ line.

17. (Currently Amended) The drive circuit according to claim 16, wherein said first, second and fourth power supply potentials are the same potential ~~(VDD)~~, and

said third and fifth power supply potentials are the same potential ~~(GND)~~.

18. (Currently Amended) The drive circuit according to claim 16, wherein said first, second and fifth power supply potentials are the same potential ~~(VDD)~~, and

said third and fourth power supply potentials are the same potential ~~(GND)~~.

19. (Currently Amended) The drive circuit according to claim 1, wherein said first differential amplifier ~~(21)~~ includes:

seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6)~~ having gates receiving said input potential ~~(VI)~~ and a potential at said second ~~first~~ node ~~(N9)~~, respectively, and first electrodes connected to each other;

first and second resistors ~~(22, 23)~~ connected between a fourth power supply potential ~~(VDD)~~ line and second electrodes of said seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6)~~, respectively; and

a current limiting element ~~(7)~~ connected between the first electrodes of said seventh and eighth ~~fourth and fifth~~ transistors ~~(5, 6)~~, respectively, and a fifth power supply potential ~~(GND)~~ line.

20. (Currently Amended) The drive circuit according to claim 1, wherein each of said first to sixth ~~thirst~~ transistors ~~(8-10)~~ is a thin film transistor.